HTS140P03 P-1

30V P-Ch Power MOSFET

V_{DS}		-30	V
$R_{DS(on),typ}$	V_{GS}=10V	12	mΩ
$R_{DS(on),typ}$	V_{GS}=4.5V	17	mΩ

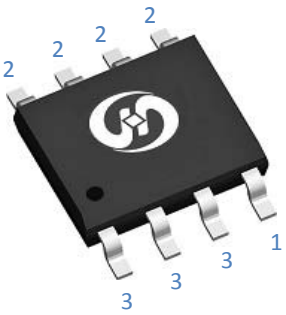
Feature

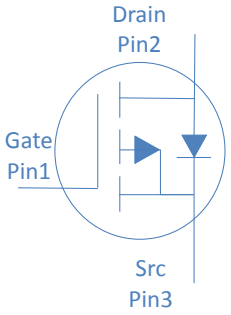
- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Application

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial

SOIC-8





Part Number	Package	Marking
HTS140P03	SOIC-8	TS140P03

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	-12	A
Drain to Source Voltage	V_{DS}		-30	
Gate to Source Voltage	V_{GS}	-	±25	V
Pulsed Drain Current	I_{DM}		-48	A
Avalanche Energy, Single Pulse	E_{AS}			
			2.5	W
			-55 to150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	℃/W

Electrical Characteristics at T_j=25°C (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250µA	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250µA	-1.0	-1.5	-3.0	
Zero Gate Voltage Drain Current	I_{DSS}					
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-12A	-	12	14	mΩ
Transconductance						
			-	2270		
Output Capacitance	C_{oss}		-			
			-	300	-	
					-	
Gate to Source Charge			-	4.9	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	7.5		
				15		

Fig 1. Typical Output Characteristics

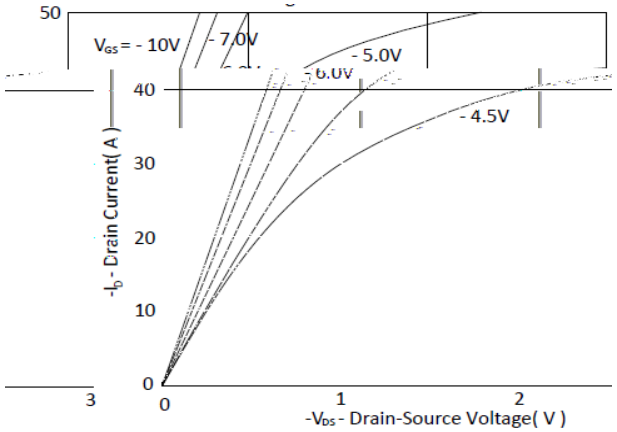


Figure 2. On-Resistance vs. Gate-Source Voltage

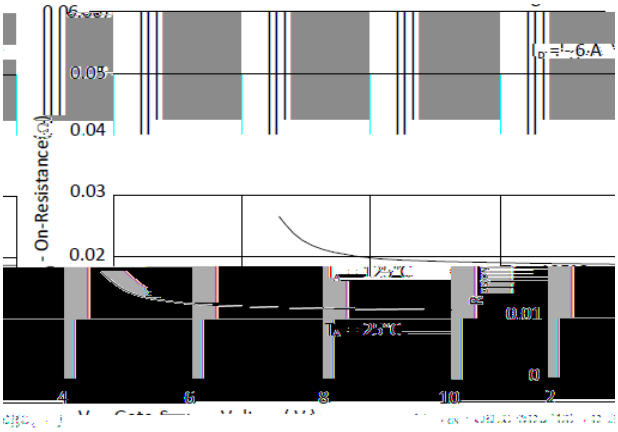


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

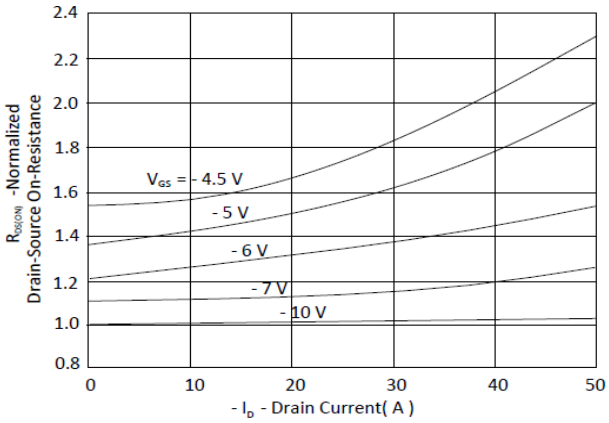


Figure 4. Normalized On-Resistance vs. Junction Temperature

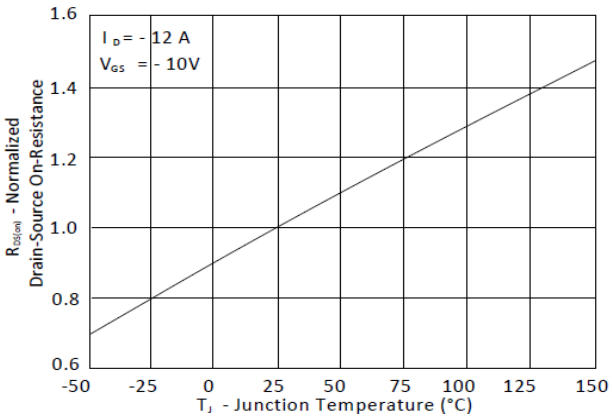


Figure 5. Typical Transfer Characteristics

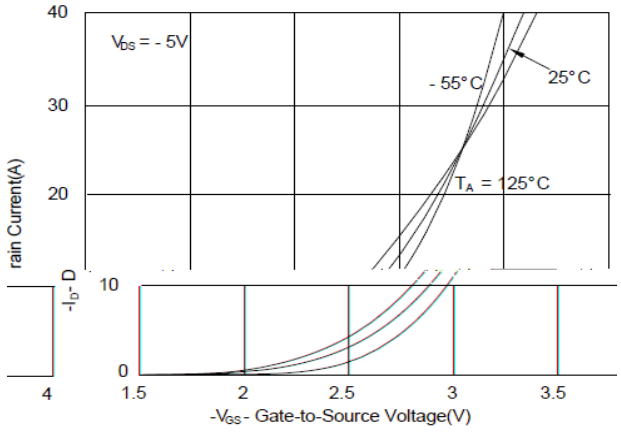


Figure 6. Typical Source-Drain Diode Forward Voltage

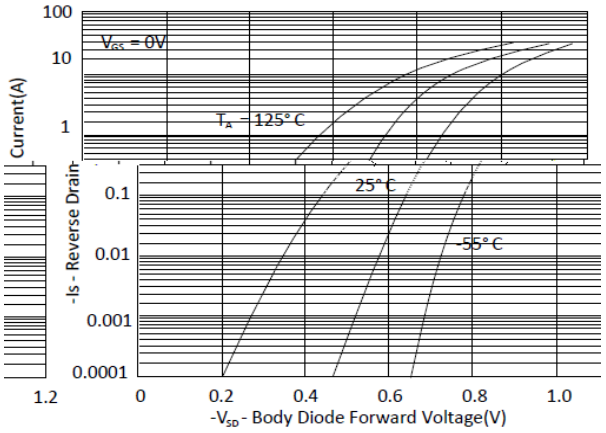


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

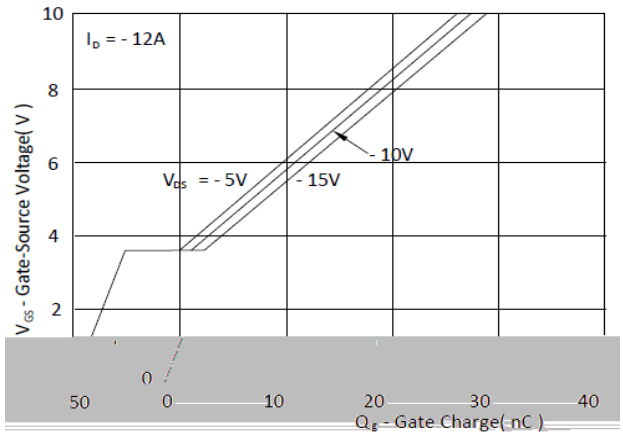


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

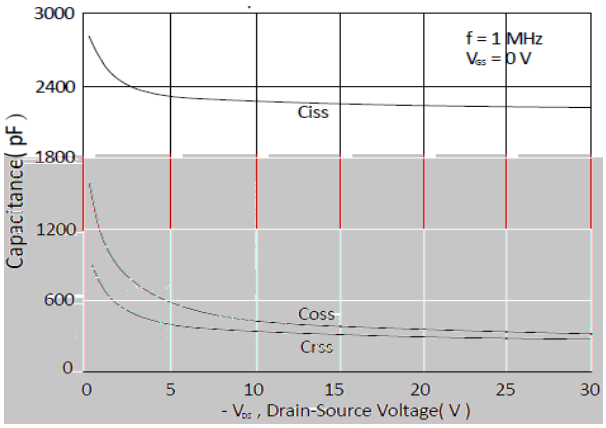


Figure 9. Maximum Safe Operating Area

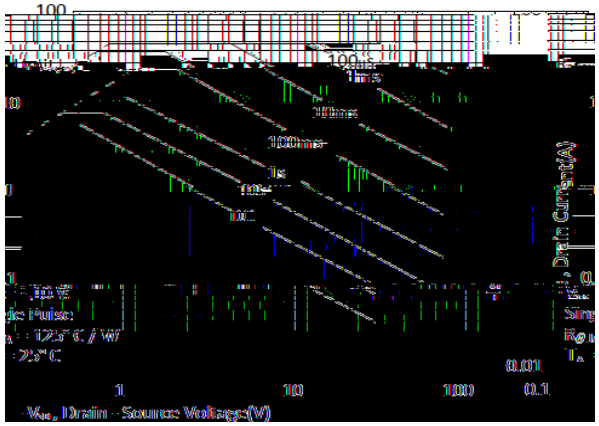


Figure 10. Single Pulse Maximum Power Dissipation

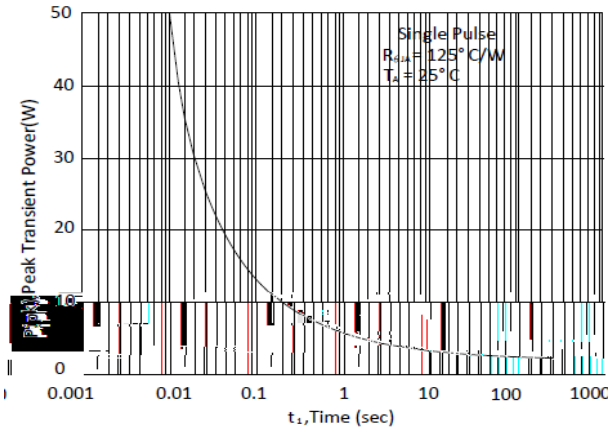
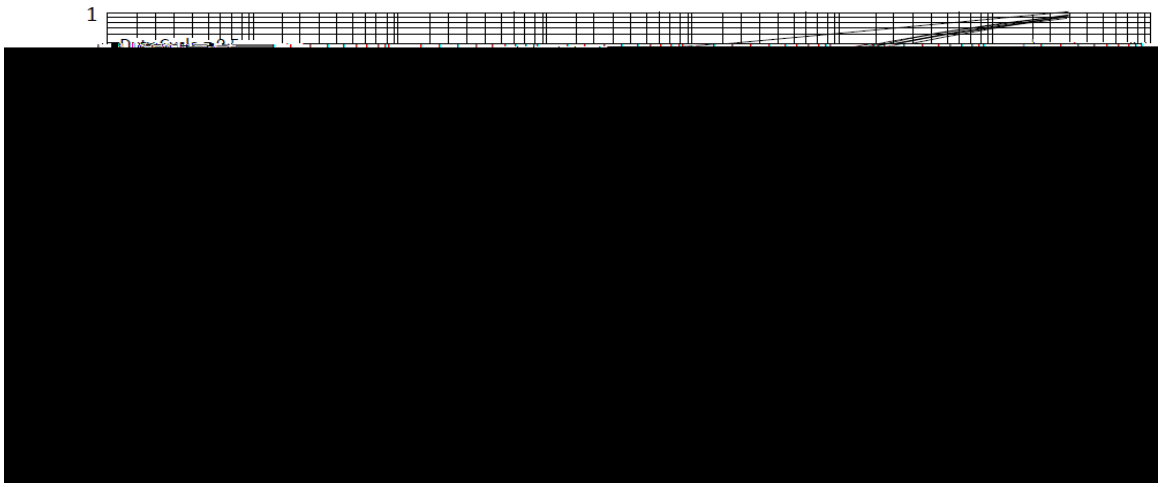


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	

Diode Recovery Test	

Package Outline

SOP-8, 8leads